ABSTRACT

A method and system for testing a plurality of cores in an integrated circuit is disclosed. The method and system include providing a plurality of slave controllers a master controller. Each of the plurality of slave controllers is for testing at least one of the plurality of cores. The master controller is coupled with the plurality of slave controllers in a star configuration. The master controller is configured to allow test data to be input directly to a portion of the plurality of slave controllers in parallel. The portion of the plurality of slave controllers can include more than one slave controller.